# Solution of HW-Lecture 1 & 2

1. Convert the following unsigned binary numbers to decimal and hexadecimal.

(a) 10102 (b) 111100002

**Solution：**(a) 10（10），A（16） (b) 240（10） ，F0（16）

1. Convert the following two’s complement binary numbers to decimal.

(a) 1101102 (b) 011100002 (c) 100111112

**Solution：**(a) -10 (b) 112 (c)-97

1. What are the largest and smallest 32-bit binary number(show the decimal values ) that can be represented with
2. unsigned numbers?
3. two’s complement numbers?
4. sign/magnitude numbers?

**Solution：**

(a) 4,294,967,295（232-1） 0

(b) 2,147,483,647（231-1） -2,147,483,648（-231）

(c) 2,147,483,647（231-1） -2,147,483,647（-231+1）

1. Convert the following decimal numbers to 8-bit two’s complement numbers or indicate that the decimal number would overflow the range.

(a) 4210 (b) −6310 (c) 12410 (d) −12810 (e) 13310

**Solution：**(a) 00101010; (b) 11000001; (c) 01111100; (d) 10000000; (e) overflow

1. extend the following 4-bit two’s complement numbers to 8-bit two’s complement numbers.

(a) 01012 (b) 10102

Repeat your work if the numbers are unsigned

**Solution：**(a) 00000101; (b) 11111010

Unsigned: (a) 00000101; (b) 00001010

1. Perform the following additions of unsigned binary numbers. Indicate whether the sum overflows an 8-bit result.

(a) 100110012 + 010001002 (b) 110100102 + 101101102

Repeat your work, assuming that the binary numbers are in two’s complement form.

**Solution：**(a) 11011101; (b) 110001000 (overflows)

two’s complement form: (a) 11011101; (b) 110001000

1. Convert the following decimal and hexadecimal numbers to 8-bit two’s complement binary numbers and add them. Indicate whether the sum overflows an 8-bit result.

(a) 2710 + 3110 (b) −410 + 1910 (c) −2810 + (-11110)(d) 8F16 + AD16

**Solution：**

(a) 00011011 + 00011111 = 00111010;

(b) 11111100 + 00010011 = 00001111;

(c) 11100100 + 10010001 = 01110101（overflow）

(d) 10001111 + 10101101 =00111100（overflow）

1. In a ***binary coded decimal*** (***BCD***) system, 4 bits are used to represent a decimal digit from 0 to 9. For example, 3710 is written as 00110111BCD.

(a) Write 37110 in BCD.

(b) Convert 000110000111BCD to decimal.

(c) Convert 10010101BCD to binary.

(d) Explain the disadvantages of BCD when compared with binary representations of numbers.

**Solution：**

(a) 0011 0111 0001

(b) 187

(c) 95 = 1011111   
(d) Addition of BCD numbers doesn't work directly. Also, the representa tion doesn't maximize the amount of information that can be stored; for example 2 BCD digits requires 8 bits and can store up to 100 values (0-99) - unsigned 8 bit binary can store 28 (256) values.

1. Is it possible to assign logic levels so that a device with the transfer characteristics shown in Figure 1.1 would serve as a buffer? If so, what are the input and output low and high levels (VIL, VOL, VIH, and VOH) and noise margins (NML and NMH)? If not, explain why not.



Figure 1.1 Figure 1.1 DC transfer characteristics

**Solution：**

The device must be able to actually produce the desired output levels. Thus, VOL can be no lower than 1V，VOH can be no higher than 4.5V

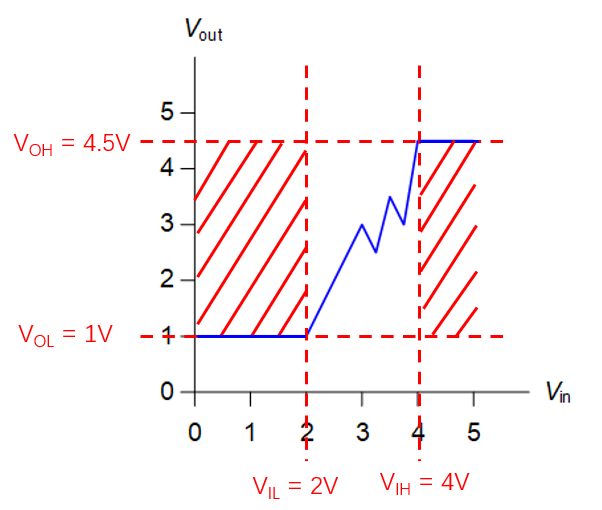
Try VOL = 1V, VOH= 4.5V

VIL must be low enough to produce VOL and VIH must be high enough to produce VOL

Try VIL = 2V, VIH = 4V

We verify that VOUT ≥ VOH when VIN ≥ VIH and VOUT ≤ VOL when VIN ≤ VIL.

Ploting these thresholds on the graph and adding forbidden regions, we see that VTC is legal.

So the device can be used as a buffer when VOL = 1V, VOH= 4.5V, VIL = 2V,

VIL = 4V. Now noise margins are

NML = VIL - VOL = 2 – 1 = 1V

NMH = VOH – VIH = 4.5 – 4 = 0.5V

1. Ben Bitdiddle has invented a circuit with the transfer characteristics shown in Figure 1.2 that he would like to use as a buffer. Will it work? Why or why not? He would like to advertise that it is compatible with LVCMOS and LVTTL logic. Can Ben’s buffer correctly receive inputs from those logic families? Can its output properly drive those logic families? Explain.



Figure 1.2 Ben’s buffer DC transfer characteristics

**Solution：**The circuit functions as a buffer with logic levels VIL = 1.5; VIH = 1.8; VOL = 1.2; VOH = 3.0. It can receive inputs from LVCMOS and LVTTL gates because their output logic levels are compatible with this gate’s input levels. However, it cannot drive LVCMOS or LVTTL gates because the 1.2 VOL exceeds the VIL of LVCMOS and LVTTL.

1. The following are voltage transfer characteristics of single-input, single-output devices to be used in a new logic family:

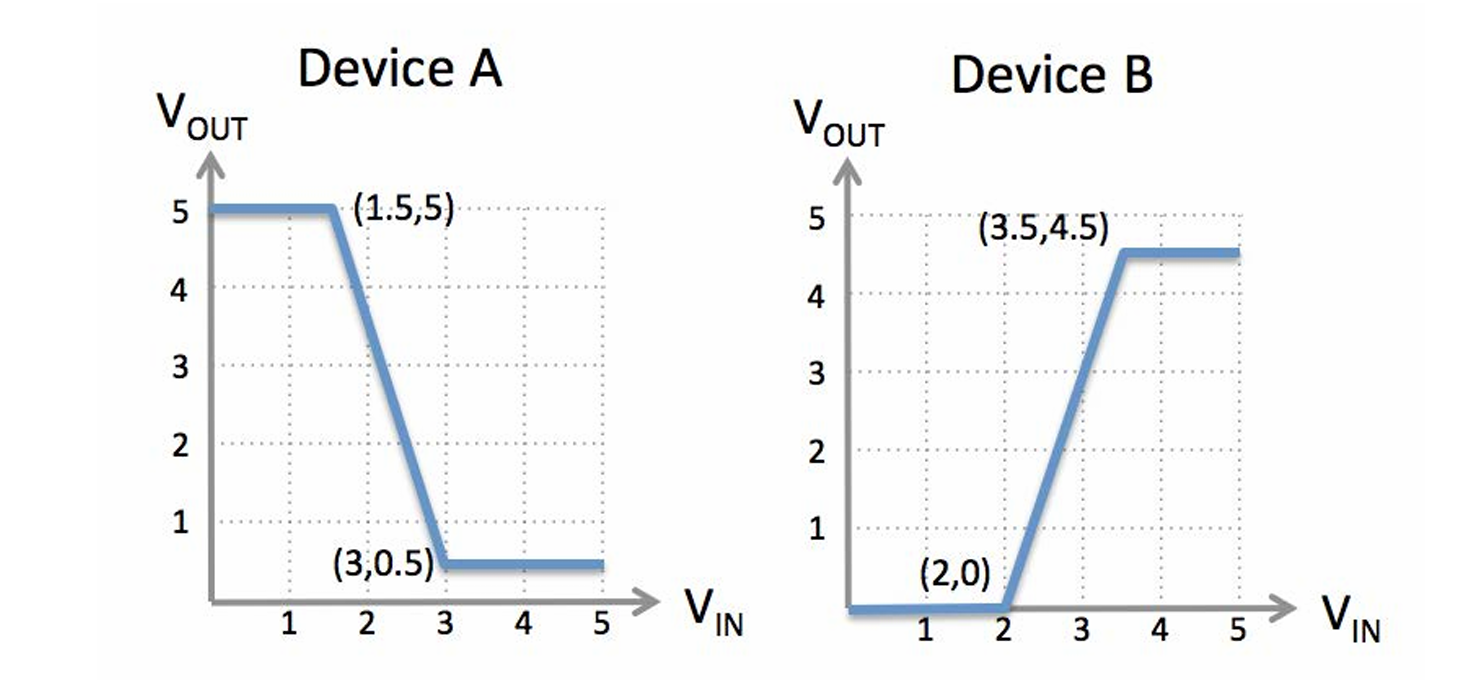


Figure 1.3 DC transfer characteristics of new logic family devices

Your job is to choose a single set of signaling thresholds VOL, VIL, VOH, and VIH to be used with both devices to give the best noise margins you can.

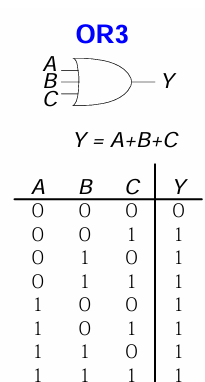
**Solution：**

VOL = \_\_0.5V \_\_ VIL = \_1.5V \_ VIH = \_\_3.5V \_ VOH = \_4.5V \_\_

Low Noise Margin = \_1V \_

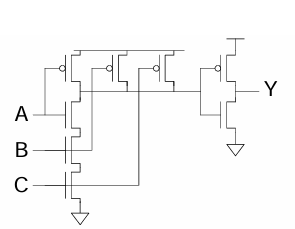
High Noise Margin = \_1V \_

1. Draw the symbol, Boolean equation, and truth table for a three-input OR gate.

**Solution：**

1. Sketch a transistor-level circuit for a three-input AND gate, use a minimum number of transistors.

**Solution：**



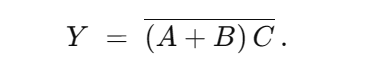
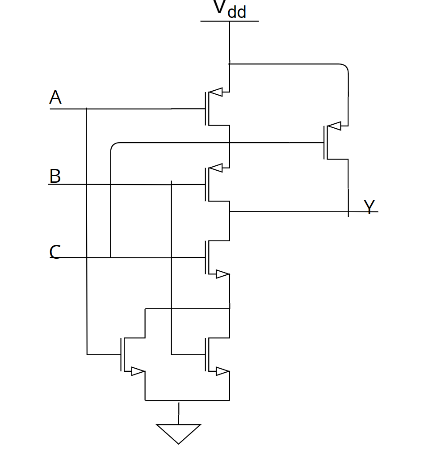
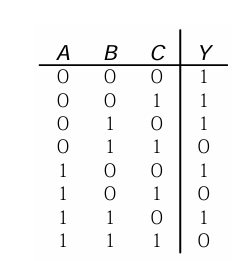
1. A three-input OR-AND-INVERT (OAI) gate shown in Figure 1.4 produces a FALSE output if C is TRUE and A or B is TRUE. Otherwise, it produces a TRUE output. Complete a truth table for the gate.



Figure 1.4 OAI

Sketch a transistor-level circuit for this CMOS gates. Use a minimum number of transistors.

**Solution：**

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1. Write a truth table for the function performed by the gate in Figure 1.5. The truth table should have two inputs, A and B. What is the name of this function?



Figure 1.5

**Solution：**

